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Power MOSFET, 72 A



SOT-227

FEATURES

- Fully isolated package
- Easy to use and parallel
- Low on-resistance
- Dynamic dV/dt rating
- Fully avalanche rated
- Simple drive requirements
- Low gate charge device
- Low drain to case capacitance
- Low internal inductance
- UL approved file E78996
- Designed for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRODUCT SUMMARY	
V_{DSS}	500 V
$R_{DS(on)}$	61.5 mΩ
I_D	72 A
Type	Modules - MOSFET
Package	SOT-227

DESCRIPTION

Third Generation Power MOSFETs from Vishay Semiconductors provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 600 W to 1000 W. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at V_{GS} 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	72	A
		$T_C = 90\text{ }^\circ\text{C}$	52	
Pulsed drain current	$I_{DM}^{(1)}$		228	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	1136	W
		$T_C = 90\text{ }^\circ\text{C}$	545	
Gate to source voltage	V_{GS}		± 20	V
Single pulse avalanche energy	$E_{AS}^{(2)}$		725	mJ
Repetitive avalanche current	$I_{AR}^{(1)}$		22	A
Repetitive avalanche energy	$E_{AR}^{(1)}$		120	mJ
Peak diode recovery dV/dt	dV/dt ⁽³⁾		10	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	°C
Insulation withstand voltage (AC-RMS)	V_{ISO}		2.5	kV
Mounting torque		M4 screw, on terminals and heatsink	1.3	Nm

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 18)
 (2) Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 500\text{ }\mu\text{H}$, $R_g = 2.4\text{ }\Omega$, $I_{AS} = 57\text{ A}$ (see fig. 18)
 (3) $I_{SD} \leq 57\text{ A}$, $dI_F/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150\text{ }^\circ\text{C}$

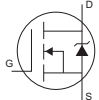


THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T_J, T_{Stg}		- 55	-	150	°C
Junction to case	R_{thJC}		-	-	0.11	°C/W
Case to heatsink	R_{thCS}	Flat, greased surface	-	0.05	-	
Weight			-	30	-	g
Mounting torque			-	-	1.3	Nm
Case style			SOT-227			

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ °C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to $25\text{ °C}, I_D = 1\text{ mA}$	-	0.64	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}^{(1)}$	$V_{GS} = 10\text{ V}, I_D = 34\text{ A}$	-	61.5	80.0	mΩ
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	3.0	4.0	V
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}, T_J = 125\text{ °C}$	-	1.9	-	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 34\text{ A}$	-	52.5	-	S
Drain to source leakage current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	0.5	50	μA
		$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	30	500	
		$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$	-	0.2	3.0	mA
Gate to source forward leakage	I_{GSS}	$V_{GS} = 20\text{ V}$	-	-	200	nA
Gate to source reverse leakage		$V_{GS} = -20\text{ V}$	-	-	- 200	
Total gate charge	Q_g	$I_D = 60\text{ A}$ $V_{DS} = 400\text{ V}$ $V_{GS} = 10\text{ V}$; see fig. 15 and 19 ⁽¹⁾	-	225	338	nC
Gate to source charge	Q_{GS}		-	51	77	
Gate to drain ("Miller") charge	Q_{gd}		-	98	147	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ $I_D = 60\text{ A}$ $R_g = 2.4\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$; diode used: 60APH06	-	134	-	ns
Rise time	t_r		-	44	-	
Turn-off delay time	$t_{d(off)}$		-	150	-	
Fall time	t_f		-	43	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ $I_D = 60\text{ A}$ $R_g = 2.4\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$; diode used: 60APH06	-	135	-	ns
Rise time	t_r		-	47	-	
Turn-off delay time	$t_{d(off)}$		-	160	-	
Fall time	t_f		-	35	-	
Internal source inductance	L_S	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 14	-	10 000	-	pF
Output capacitance	C_{oss}		-	1500	-	
Reverse transfer capacitance	C_{rss}		-	50	-	

Note

⁽¹⁾ Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	72	A
Pulsed source current (body diode)	$I_{SM}^{(1)}$		-	-	228	
Diode forward voltage	$V_{SD}^{(2)}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 57\text{ A}, V_{GS} = 0\text{ V}$	-	0.9	1.31	V
		$T_J = 125\text{ }^\circ\text{C}, I_S = 57\text{ A}, V_{GS} = 0\text{ V}$	-	0.75	-	
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 50\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}^{(2)}$	-	660	-	ns
Reverse recovery current	I_{rr}		-	46	-	A
Reverse recovery charge	Q_{rr}		-	15	-	μC
Reverse recovery time	t_{rr}	$T_J = 125\text{ }^\circ\text{C}, I_F = 50\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}^{(2)}$	-	880	-	ns
Reverse recovery current	I_{rr}		-	50	-	A
Reverse recovery charge	Q_{rr}		-	23	-	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- (2) Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

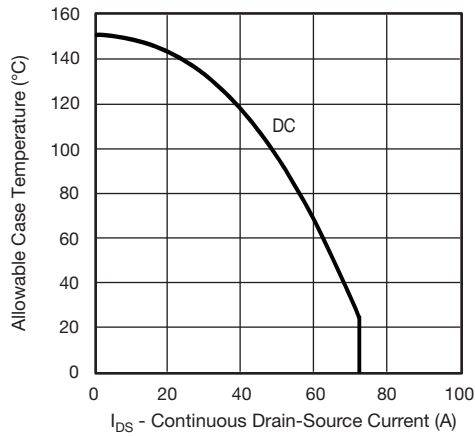


Fig. 1 - Maximum DC MOSFET Drain-Source Current I_{DS} (A)

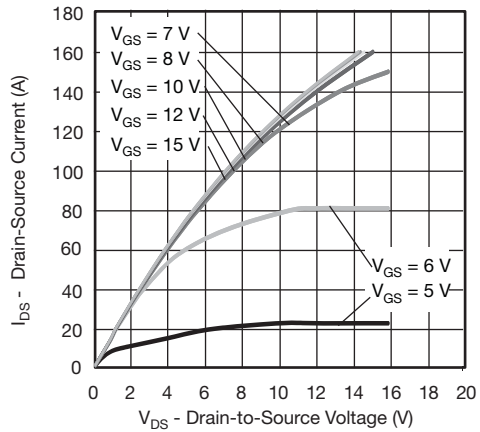


Fig. 3 - Typical Drain-to-Source Output Characteristics at $T_J = 25\text{ }^\circ\text{C}$

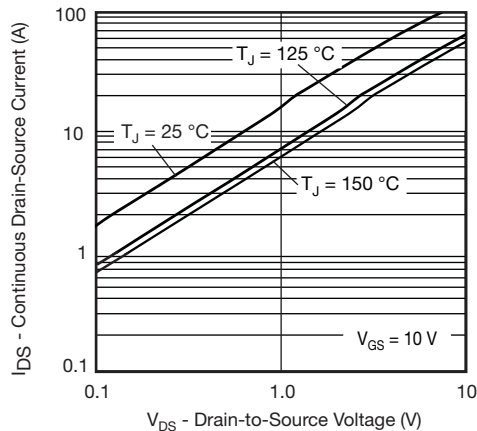


Fig. 2 - Typical Drain-to-Source Output Characteristics

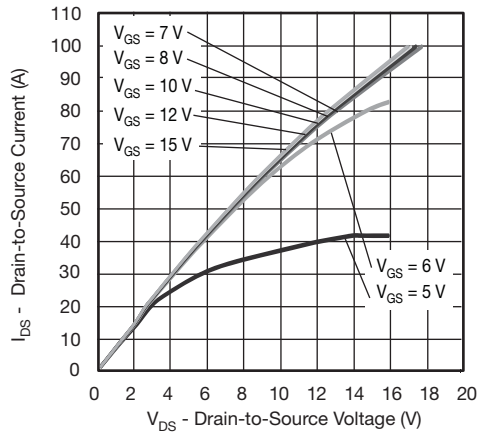


Fig. 4 - Typical Drain-to-Source Current Output Characteristics at $T_J = 125\text{ }^\circ\text{C}$

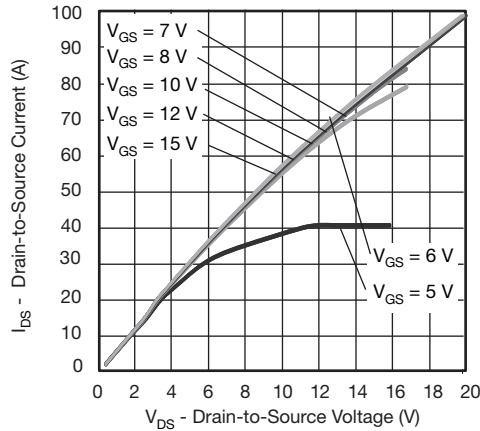


Fig. 5 - Typical Drain-to-Source Current Output Characteristics at $T_J = 150^\circ\text{C}$

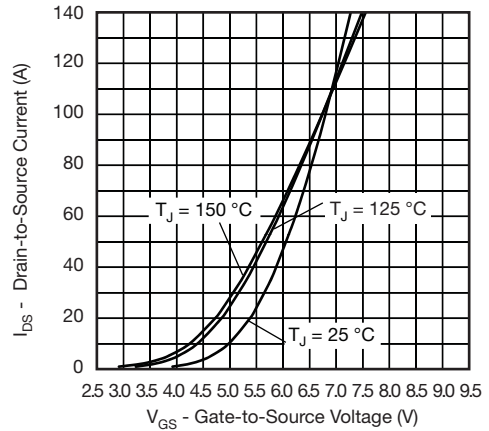


Fig. 8 - Typical MOSFET Transfer Characteristics

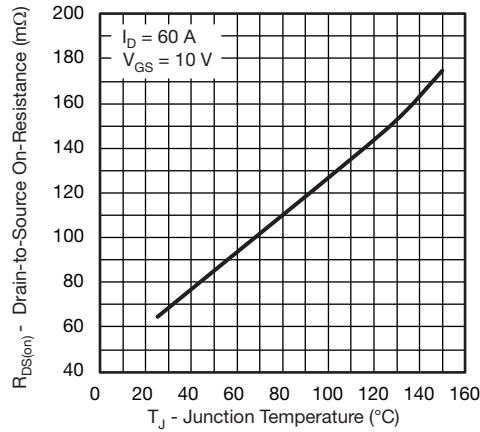


Fig. 6 - Typical Drain-to-Source On-Resistance vs. Temperature

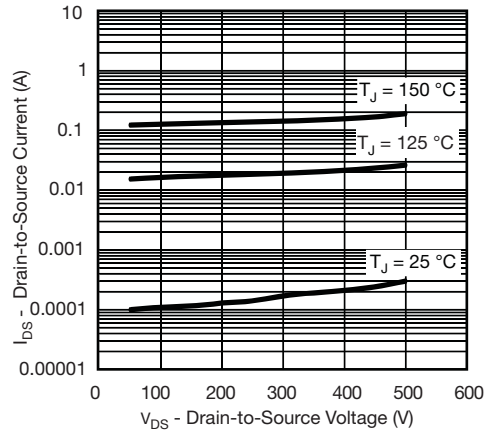


Fig. 9 - Typical MOSFET Zero Gate Voltage Drain Current

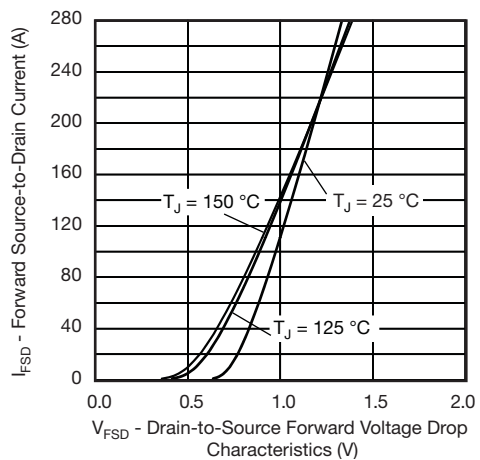


Fig. 7 - Typical Body Diode Forward Voltage Drop Characteristics

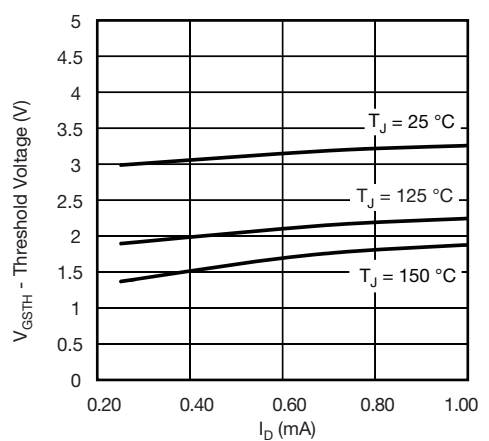


Fig. 10 - Typical MOSFET Threshold Voltage

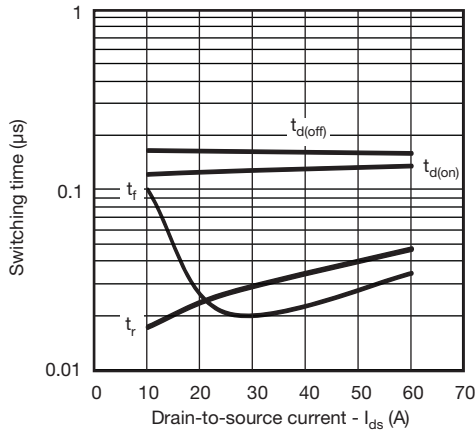


Fig. 11 - Typical MOSFET Switching Time vs. I_{DS} , $T_J = 125^\circ\text{C}$, $V_{DD} = 250\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 500\ \mu\text{H}$, $R_G = 2.4\ \Omega$
Diode used: 60APH06

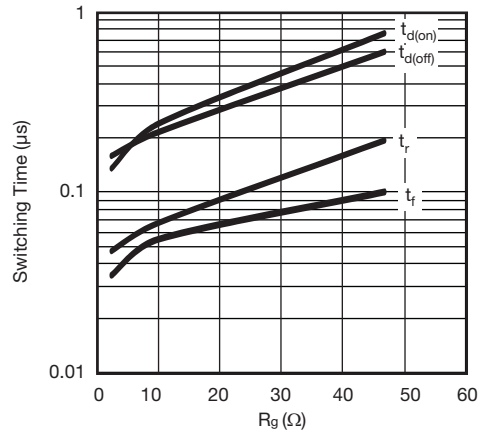


Fig. 12 - Typical MOSFET Switching Time vs. R_G , $T_J = 125^\circ\text{C}$, $I_{DS} = 100\text{ A}$, $V_{DD} = 250\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 500\ \mu\text{H}$
Diode used: 60APH06

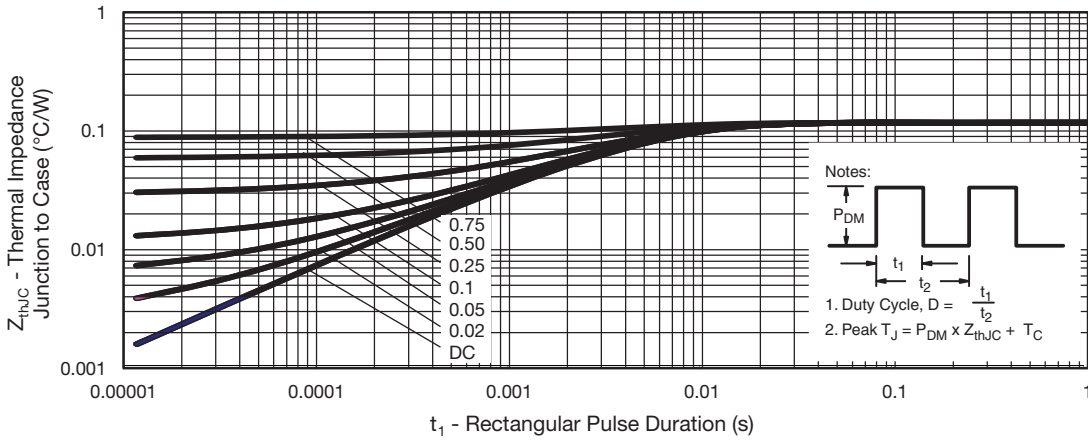


Fig. 13 - Maximum Thermal Impedance Z_{thJC} Characteristics, MOSFET

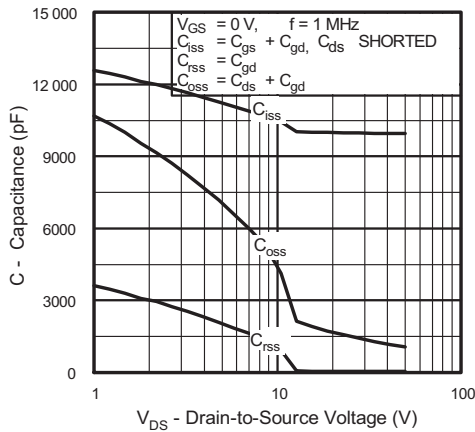


Fig. 14 - Typical Capacitance vs. Drain-to-Source Voltage

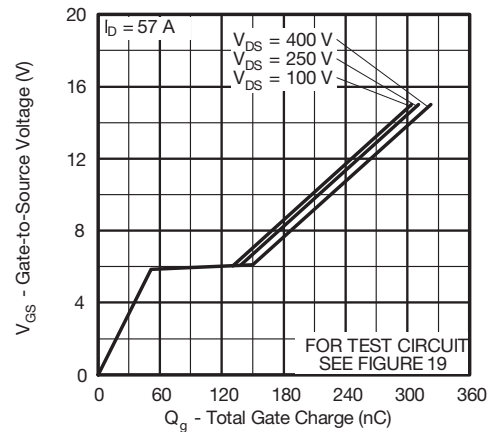


Fig. 15 - Typical Gate Charge vs. Gate-to-Source Voltage

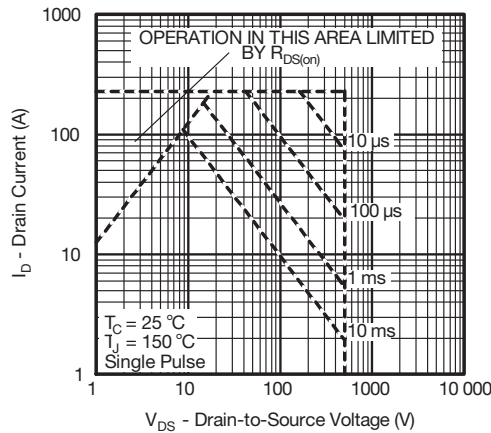


Fig. 16 - Maximum Safe Operating Area

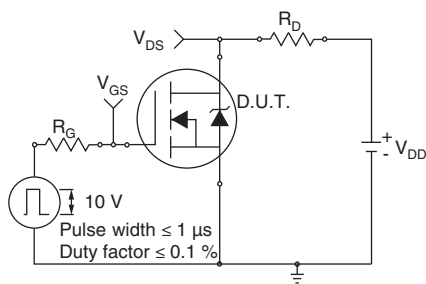


Fig. 17a - Switching Time Test Circuit

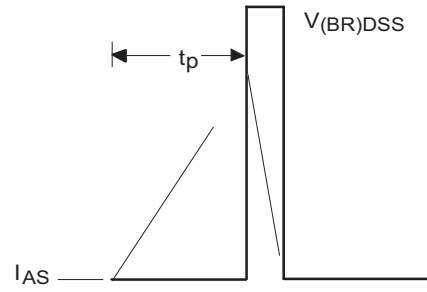


Fig. 18b - Unclamped Inductive Waveforms

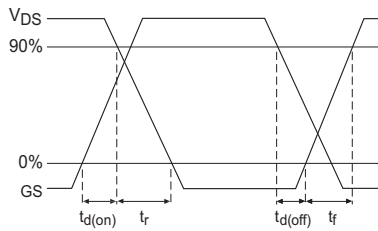


Fig. 17b - Switching Time Waveforms

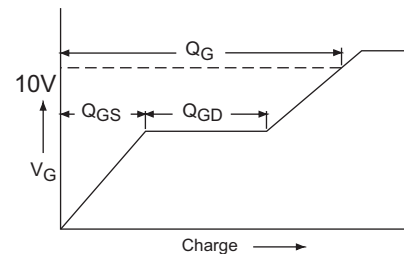


Fig. 19a - Basic Gate Charge Waveform

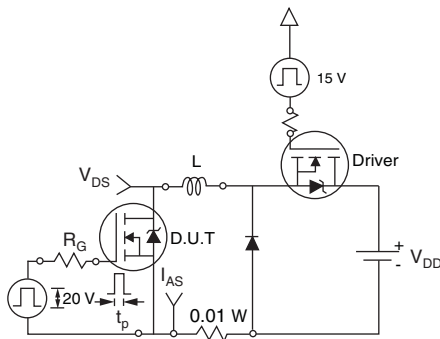


Fig. 18a - Unclamped Inductive Test Circuit

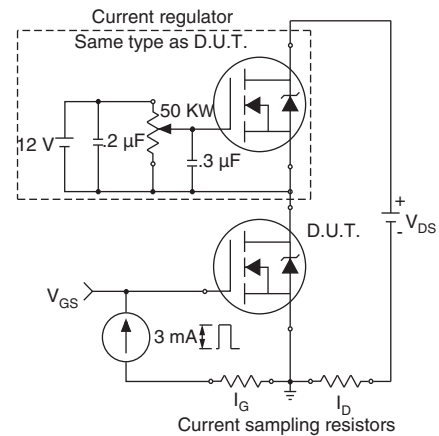


Fig. 19b - Gate Charge Test Circuit

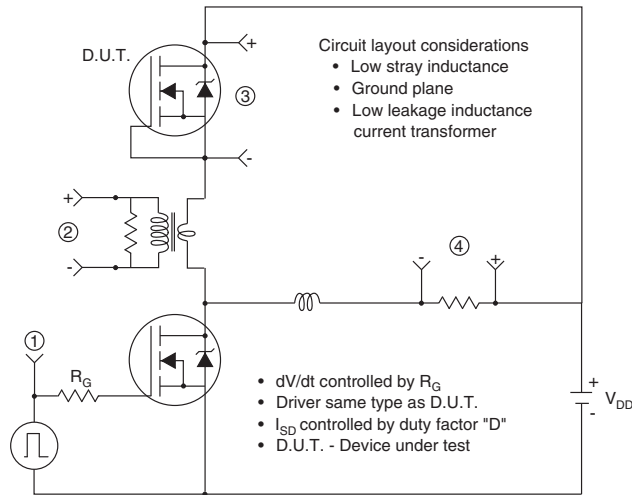
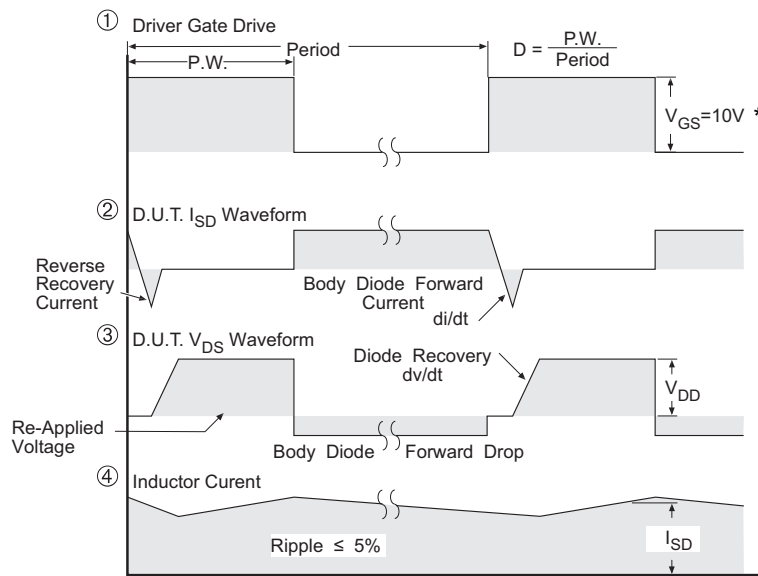


Fig. 19c - Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig. 20 - For N-Channel Power MOSFETs

ORDERING INFORMATION TABLE

Device code	VS-	F	A	72	S	A	50	LC
	①	②	③	④	⑤	⑥	⑦	⑧

- 1** - Vishay Semiconductors product
- 2** - Power MOSFET
- 3** - A = Generation 3, MOSFET silicon die
- 4** - Current rating (72 = 72 A)
- 5** - Single switch
- 6** - Package indicator (SOT-227)
- 7** - Voltage rating (50 = 500 V)
- 8** - LC = Low charge

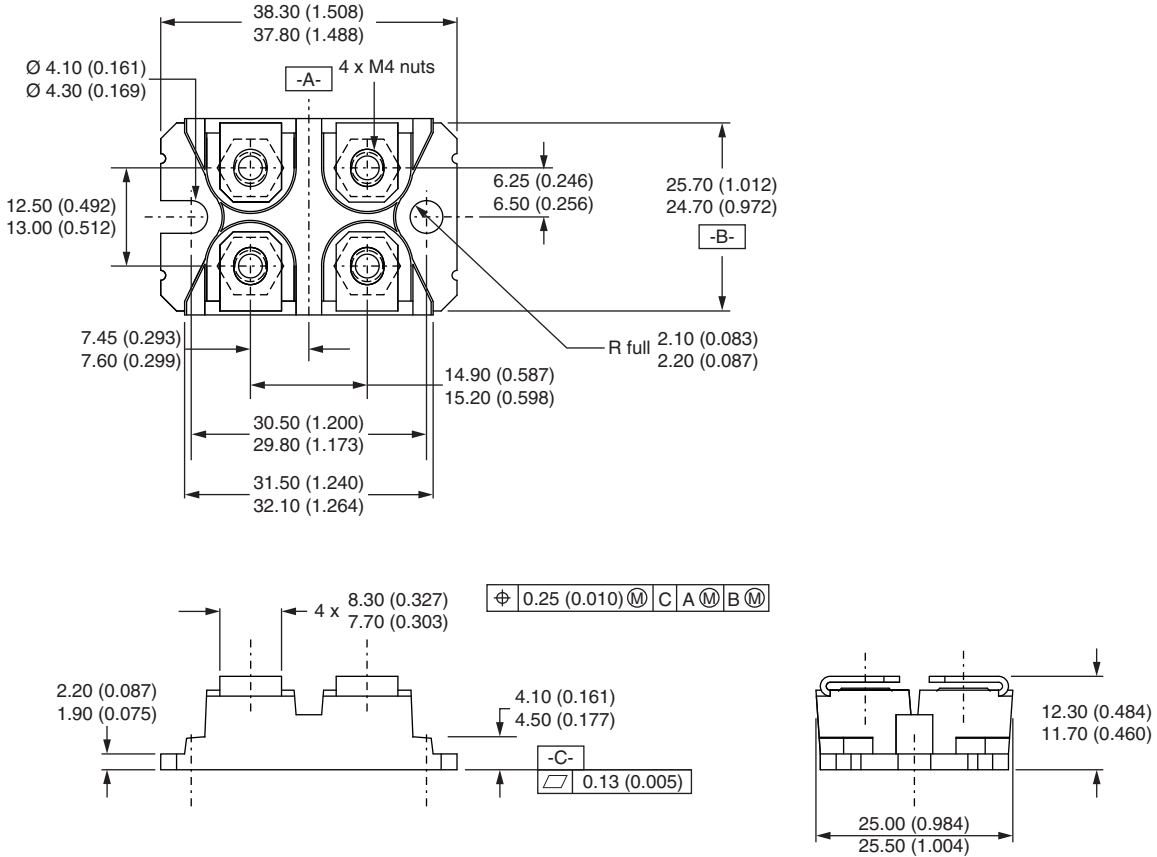
CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch	S	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95423
Packaging information	www.vishay.com/doc?95425



SOT-227 Generation II

DIMENSIONS in millimeters (inches)



Note

- Controlling dimension: millimeter



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